REMARKS

This paper is responsive to the Non-Final Office action dated October 20, 2003. Claims 1-68 were examined, and all claims were rejected.

Claims 1-6, 13-16, 24-34, 50 and 63 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Krentz, et al. (U.S. Patent No. 5,371,706). Applicant respectfully traverses this rejection.

Krentz describes a programmable memory circuit having a wordline decoder 16 which, in the read mode, functions "in response to wordline address signals on lines 20r and to signals from Read/Write/Erase control circuit 21, to apply a preselected positive voltage Vcc (approx. +5V) to the selected wordline 15, and to apply a low voltage (ground or Vss) to deselected wordlines 15." (column 5, lines 38-44).

Krentz also describes a test mode to detect whether memory cells have been erased into a depletion mode threshold voltage. In a prior art technique depicted in Fig. 2, "all the wordlines 15 in the array are held to a user-supplied level, usually reference voltage Vss or a small positive voltage." (column 6, lines 10-12). In another prior art circuit depicted in Fig. 3, Krentz describes using a sense amplifier 25 "in a read mode to apply a voltage to both the addressed drain-column line 18A and the reference drain-column line 18R of cells 10. The sense amplifier 25 then compares the current of the two drain-column lines 18A, 18R of cells 10 to determine whether or not a cell 10 in the addressed column is programmed, the particular cell 10 having a read voltage Vcc applied to its wordline 15 and control gate 14." (column 6, lines 35-43).

Krentz also describes a circuit in accordance with his invention to detect whether memory cells have been erased into a depletion mode threshold voltage. In such a test mode, Krentz describes "[a]s in the prior art, a predetermined voltage is applied to all of the wordlines 15. The predetermined voltage may be a small positive voltage or reference voltage." (column 7, lines 5-7)

In contrast, Applicant's claim 29 recites an integrated circuit including the limitations:

> an X-line circuit *for selecting*, in a first mode of operation, an X-line associated with a first selected Y-line to impress *a read bias* across a corresponding memory cell coupled between the selected X-line and the first selected Y-line, and *for selecting*, in a second mode of operation, a first plurality of X-lines associated with the first selected Y-line to impress *a read bias* across each of a corresponding first plurality of selected memory cells respectively coupled between the first plurality of selected X-lines and the first selected Y-line; (Claim 29, lines 6-12)

Krentz does not teach or suggest a circuit which during the second mode *selects* a plurality of wordlines to impress *a read bias* across a corresponding plurality of memory cells, as recited in the claim. Rather, Krentz describes a test mode in which all the wordlines are taken to a voltage (e.g., a reference voltage Vss or a slight positive voltage) which more accurately corresponds to the voltage to which the *unselected* wordlines are taken in the read mode (see above). Such is not a read bias. By his own statements, Krentz essentially *grounds all* the wordlines (or very nearly grounds them), and senses a *leakage current* on the selected drain-column line.

Applicant respectfully submits that claim 29 is allowable over the art of record.

Claims 50 and 63 were rejected under the same argument, and Applicant traverses the rejection for analogous reasons as above.

In particular, claim 50 recites an integrated circuit including the limitations:

> means for simultaneously *selecting* a plurality of memory cells arranged in at least one group of memory cells; [and]
> means for determining whether *an aggregate read current* greater than a particular value flows through the selected memory cells in each respective group;

Claim 63 recites an integrated circuit including the limitations:

> a first X-line circuit normally configured *to select* one of a first plurality of X-lines associated with a first selected Y-line but configurable, during a test mode, *to select more than one* of the X-lines associated with the first selected Y-line; and
> a first Y-line sense circuit for sensing, when enabled, a *read current* on the first selected Y-line;
> wherein, during the test mode, the X-line decoder is configured *to select more*

than one of the first plurality of X-lines when the first Y-line sense circuit is enabled.

Applicant submits that selecting a plurality of X-lines, as recited in the claims, is not the same as essentially grounding all the word lines in an array, nor is it taught or suggested by such a reference.

Regarding claim 30, the Office action argues that Krentz discloses (at column 6, lines 35-45) the limitation of "wherein the first read circuit is configured for determining, in the first mode of operation, whether a read current of the selected memory cell coupled to the selected Y-line exceeds a first mode threshold level of current." Applicant respectfully submits that this cited passage describes a prior art circuit utilizing a reference column, and in fact teaches away from the usefulness of such a reference line in determining whether memory cells are depletion mode. However, Applicant finds that Krentz describes (at column 6, lines 65-67) that preferably leakage current is measured internally via the sense amplifier 25 used in normal read mode operation.

The method claims 1-6, 13, 14-16, and 24-28 stand rejected for the same reasons as the apparatus claims above. Applicant respectfully traverses this rejection for analogous reasons as set forth above.

In particular, independent claim 1 recites the limitations:

in a first mode of operation, *selecting* an X-line associated with the first selected Y-line to impress a *read bias* across a corresponding memory cell coupled between the selected X-line and the first selected Y-line;

in a second mode of operation:

selecting a first plurality of X-lines associated with the first selected Y-line to impress a *read bias* across each of a corresponding first plurality of selected memory cells respectively coupled between the first plurality of selected X-lines and the first selected Y-line;

enabling a first read circuit having an input coupled to the first selected Y-line; and

generating a first read signal on an output of the first read circuit having a first value if *an aggregate read current* of the first plurality of selected memory cells exceeds a second mode threshold level.

Independent claim 14 recites the limitations:

in a first mode of operation, *selecting* an X-line associated with the first selected Y-line to impress a *read bias* across a corresponding memory cell coupled between the selected X-line and the first selected Y-line;

in a second mode of operation, *selecting a first plurality* of X-lines associated with the first selected Y-line to impress a *read bias* across each of a corresponding first plurality of selected memory cells respectively coupled between the first plurality of selected X-lines and the first selected Y-line;

in both the first and second modes of operation:

enabling a first read circuit having an input coupled to the first selected Y-line;

generating a first read signal on an output of the first read circuit having a first value if *an aggregate read current* through the one or more selected memory cells exceeds a respective threshold level; and

generating an output signal derived at least from the first read signal.

Independent claim 24 recites the limitations:

simultaneously *selecting a plurality* of memory cells arranged in at least one group of memory cells;

determining whether a *read current* greater than a particular value flows collectively through the selected memory cells in each respective group;

generating one or more output signals numbering less than the number of simultaneously selected memory cells, each respective output signal for indicating whether a *read current* greater than the particular value flows through one or more selected memory cells of each group of memory cells respectively associated therewith.

Applicant respectfully submits that Krentz, et al. does not disclose such limitations as selecting a plurality of X-lines or memory cells, impressing a read bias across such memory

cells, or sensing an aggregate read current through one or more selected memory cells, as recited in these various claims, for the reasons and distinctions stated above.

Claims 7-12, 17-23, 35-39, 51-60, and 64-67 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Krentz, et al. (U.S. Patent No. 5,371,706) in view of Tanaka, et al. (U.S. Patent No. 5,909,399). Applicant respectfully traverses this rejection, and submits that these claims are allowable at least for their dependence from an allowable independent claim.

Regarding claim 35, the Office action states that Krentz *inherently* discloses the recited limitations "since memory array can be divided into a plurality of columns or subarray of which, during the first and second mode, these columns or subarrays performed the tasks similarly to that of the first columns. Applicant respectfully traverses the suggestion. Inherency can only be supported if there is no other possible arrangement. A mere possibility of an arrangement will not suffice. Krentz discloses one array with a single sense amplifier 25. Such a circuit is plausible on its merits, and inherency therefore cannot be supported.

The Office action also relies on Tanaka, et al. for disclosing repeated features of each column having column lines and row lines and read circuits, each of which have physical and operational characteristics exactly like one another, and for the proposition that it would have been obvious to realize that Krentz's device would also have a second X-line circuit, a second plurality of X-lines, a second selected Y-line, a second plurality of selected memory cells, and a second read circuit, and which operate similarly to the first X-line circuit, first plurality of X-lines, first selected Y-line, first plurality of selected memory cells, and first read circuit.

Applicant submits that Krentz in combination with Tanaka does not suggest, *inter alia*, having a first and second *selected* Y-line in the memory array during the second mode of operation. Such would not be suggested merely by having multiple columns in a memory array behaving similarly.

The Office applies this reasoning to the remaining apparatus claims 36-39, 51-54, and 64-67, and to the method claims 7-12, 17-23, and 55-60 in the rejected claim group. Applicant respectfully submits that many of these dependent claims recite limitations that are nowhere taught or suggested by Krentz in combination with Tanaka, as will be described below.

Claims 40-42, 61-62, and 68 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Krentz, et al. (U.S. Patent No. 5,371,706) in view of Jacobson, et al. (U.S. Patent No. 6,499,124). Applicant respectfully traverses this rejection, and submits that these claims are allowable at least for their dependence from an allowable independent claim.

Regarding claim 40, the Office action cites Jacobson for disclosing that the memory cell used in his device is comprised of any type of non-volatile memory cells, of which include an anti-fuse type (column 9, line 67-column 10, line 5). Applicant respectfully submits that Jacobsen discloses a PLD device (see, e.g., Abstract, and throughout the specification) which is not a fully decoded memory array, and that the disclosed memory cell 710 corresponds to one or more security bits (see, e.g., column 6, lines 32-36; column 8, lines 32-48; column 9, lines 65-67). Thus, the suggestion by Jacobson that the memory cells 710 may be implemented by any type of non-volatile memory cell is not directed at a memory array at all. Applicant respectfully submits that Jacobson would not suggest that the non-volatile *memory array* transistor of Krentz be replaced by an anti-fuse memory cell.

Claims 43-49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Krentz, et al. (U.S. Patent No. 5,371,706) in view of Jacobson, et al. (U.S. Patent No. 6,499,124), and further in view of Tanaka, et al. (U.S. Patent No. 5,909,399). Applicant respectfully traverses this rejection, and submits that these claims are allowable at least for their dependence from an allowable independent claim.

Regarding claim 43, the Office action states an identical line of reasoning as for the rejection of claim 35 above, to which Applicant responds here likewise. In addition, Applicant respectfully submits that Krentz, Jacobson, and Tanaka in combination nowhere suggest an integrated circuit having, during the test mode of operation, two selected Y-lines, each in separate sub-arrays of the memory array.

Applicant respectfully also submits that many of the rejected dependent claims recite limitations that are nowhere taught or suggested by any of the art of record, and which do not fall within any of the reasons for rejection stated in the Office action.

For example, claim 12 recites the limitation of "in the second mode of operation: generating an output signal having a first value if either one or both of the first and second read signals are at their respective first values, and having a second value otherwise." Claim 19 also recites a similar limitation.

As another example, claim 13 recites the limitation of wherein "the read bias in the first mode of operation is substantially the same as in the second mode of operation."

Claim 16 recites the limitation of selecting the first plurality of X-lines by "over-riding at least one address signal to cause an X-line decoder to simultaneously select more than one X-line." Claim 42 also includes a similar limitation, reciting "means for inhibiting at least one address signal ... ."

Claim 21 recites the limitation of "in the second mode of operation: selecting a third Y-line disposed in a second sub-array of the memory array different than the first sub-array (in which the first and second selected Y-lines are disposed in the first sub-array), selecting a third plurality of X-lines associated with the third selected Y-line ... ; enabling a third read circuit having an input coupled to the third selected Y-line; and generating a third read signal on an output of the third read circuit ... ."

Claim 23 recites the limitation of "in the second mode of operation: generating a first output signal for indicating whether at least one of the first and second read signals is at its respective first value; and generating a second output signal for indicating whether at least the third read signal is at its respective first value."

Claim 26 recites the limitation of wherein at least one output signal represents memory cells of more than one group (i.e., of the simultaneously selected memory cells).

Claim 32 recites the limitation of "another read circuit different than the first read circuit for determining, in the first mode of operation, ..."

Claim 47 recites the limitation of a three-dimensional memory array having at least two memory planes of memory cells.

Claim 48 further recites the limitation of "the first X-line circuit is configurable during the test mode to select at least one of a plurality of first layer X-lines associated with the first selected Y-line, and to select at least one of a plurality of second layer X-lines also associated with the first selected Y-line."

Applicant respectfully submits that these dependent claims are allowable because such limitations are nowhere taught or suggested by the art of record, as well as for their dependence from an allowable independent claim.

In summary, claims 1-68 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Andrew C. Graham — 1-20-04 (Date)

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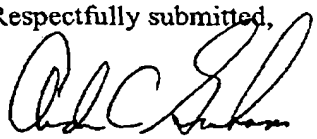

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